The Manic Depression of Microprocessor Debug

Doug Josephson

Hewlett Packard Company

Presentation Overview

- Challenges of processor debug
- Design features to support debug
- Other tools used in debugging
- Bug example
- Future challenges

Processor Debug is Hard!

- Aggressive circuit design
  - Low margin for errors
- Leading edge processes
  - Very large designs
  - Yield issues
  - Process variation is increasing
  - Lead time (masks/fabrication)
- This means... difficult debug
  - Traditional external debug methods insufficient
  - Design hooks are required for success

Internal Debug Hooks

- Debug triggers
- Scan observabililty
- Clock manipulation
- Event monitors
- Event injectors
- Hardware error checkers

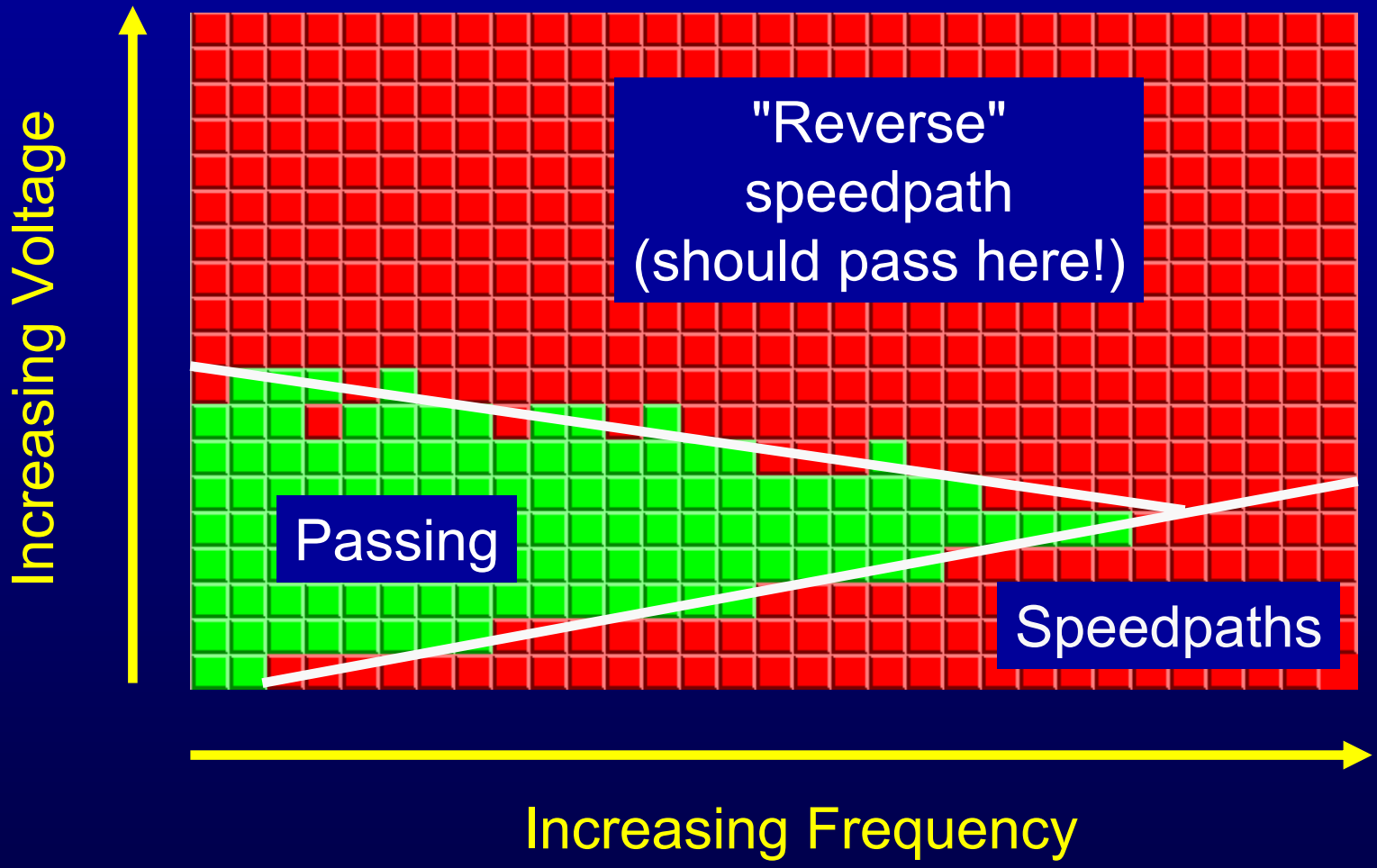
External Debug Aids

- Systems and testers
- Laser Voltage Probe (LVP) and E-beam
- Focused Ion Beam edits (FIB)
- Shmoos
- Code experimentation
  - Random
  - Manual and focused
- SPICE and other design tools

Processor Debug Example

- A failure is sourced in system testing
  - Found during OS testing
  - Isolated to driver code in the OS
- Further isolated to particular sequence
  - Back to back instructions were important
- Code sequence ported to a tester
  - Proof that failure was processor related
  - Failure was worse cold and on fast parts
  - Shmoo demonstrated a "reverse" speedpath

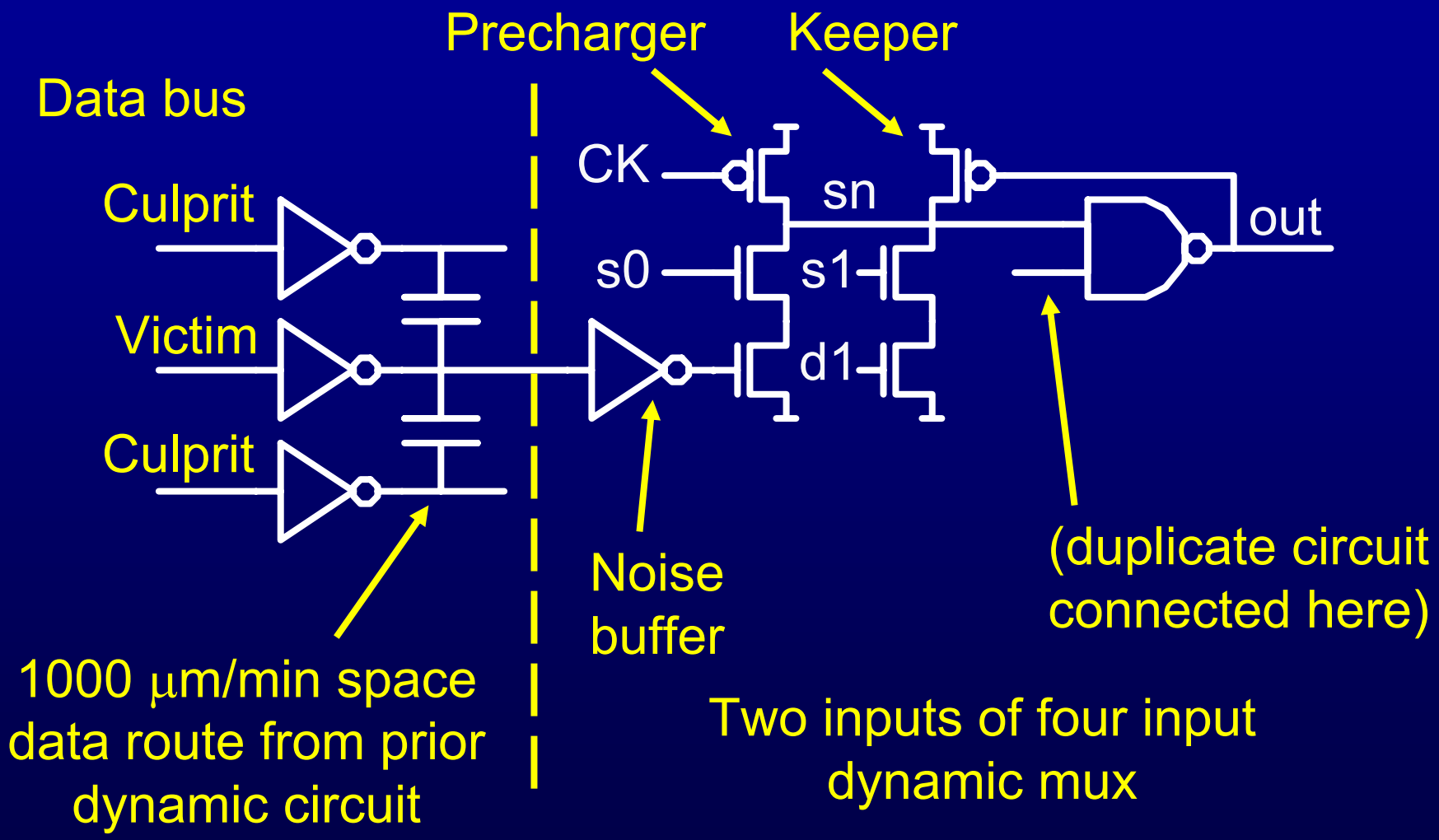
Shmoo Will Be Your Friend (?)

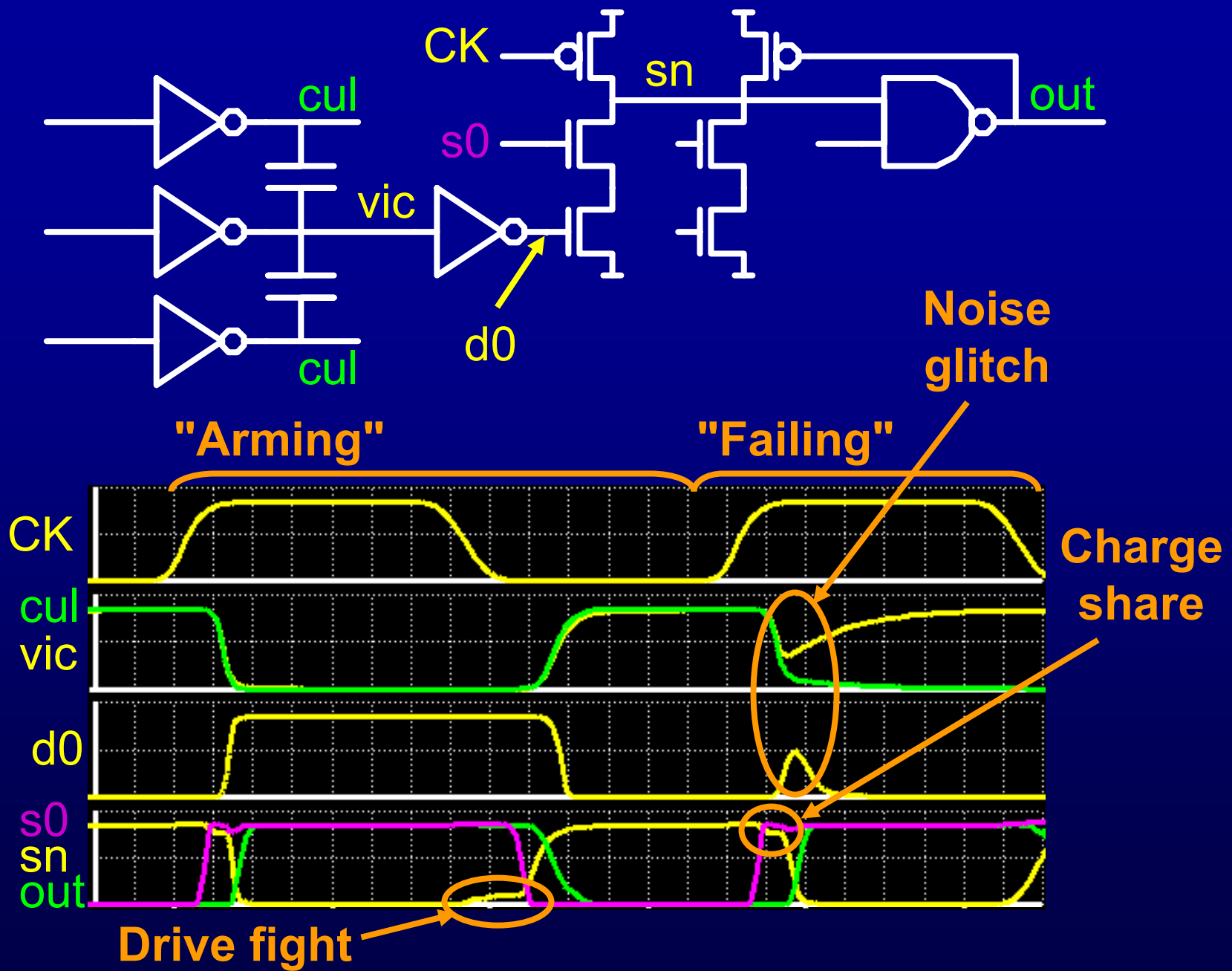


Debug Process

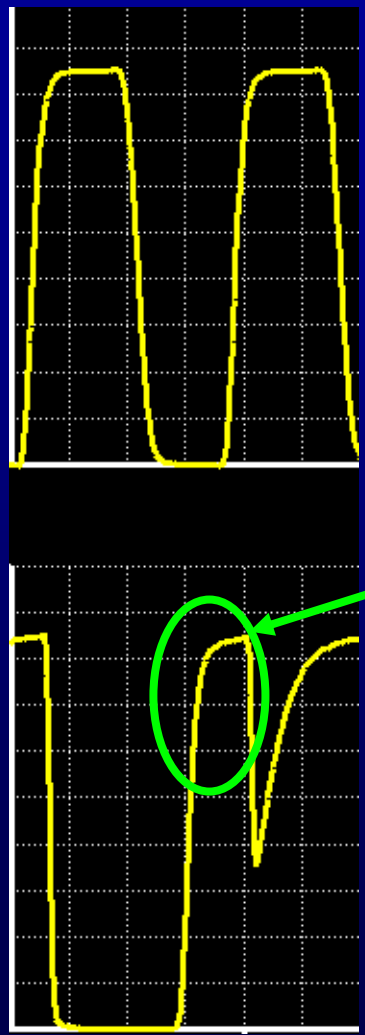
- Debug engineers begin work
  - Code/shmoo experiments
  - Scan/clock manipulation
- A suspect circuit is found
  - Based upon instructions executed by unit
  - Circuit has little noise margin
  - Circuit also has marginal precharge
  - Focus narrows to artwork/SPICE

Suspect - Dynamic Mux




CK
sn
cul
out
s0
vic
d0
cul
Noise glitch
"Arming"
"Failing"
CK
cul
vic
d0
s0
sn
out
Charge share
Drive fight

SPICE vs. Probing Results



SPICE

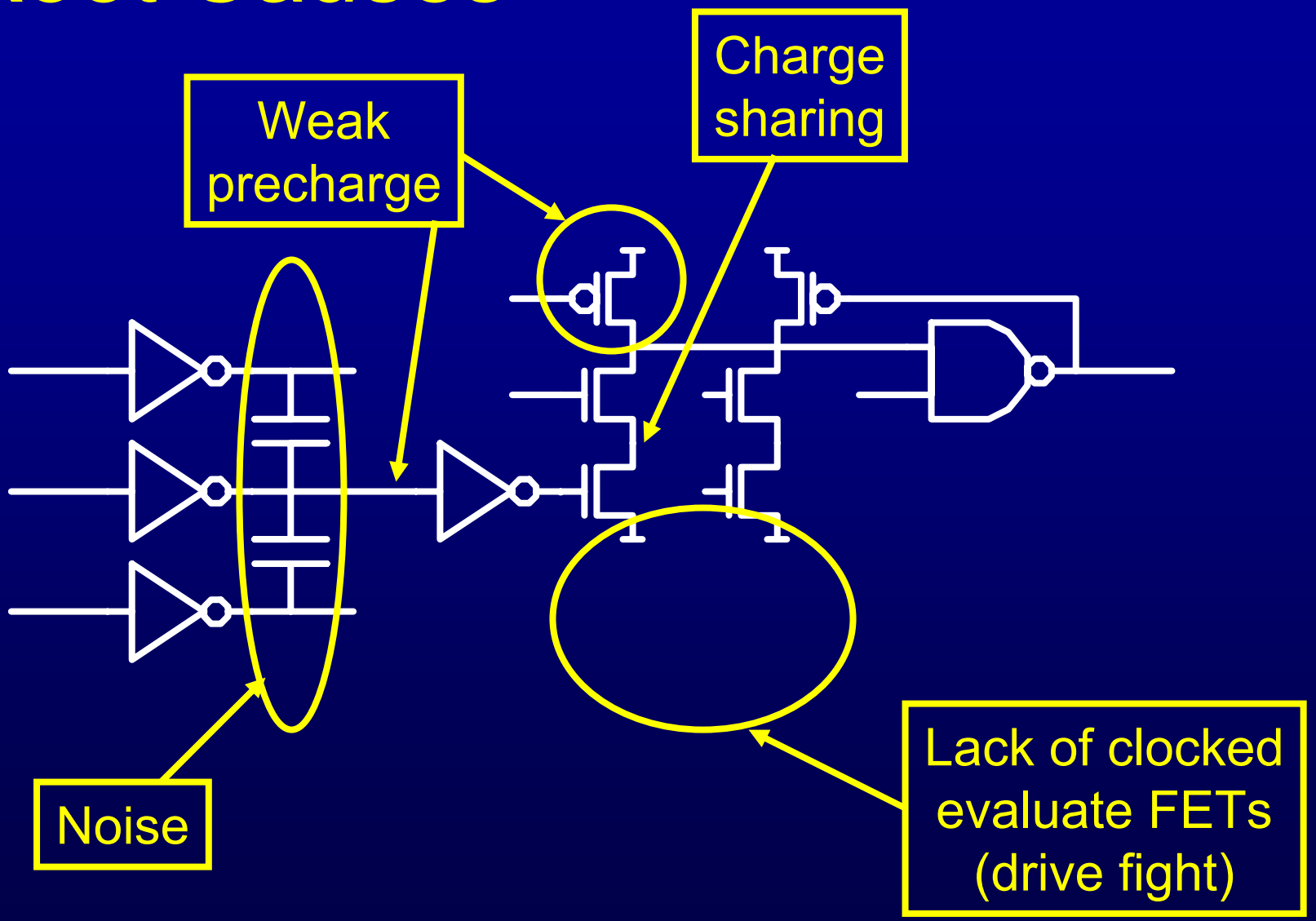
CK

Victim line (pre-mux)

Probing

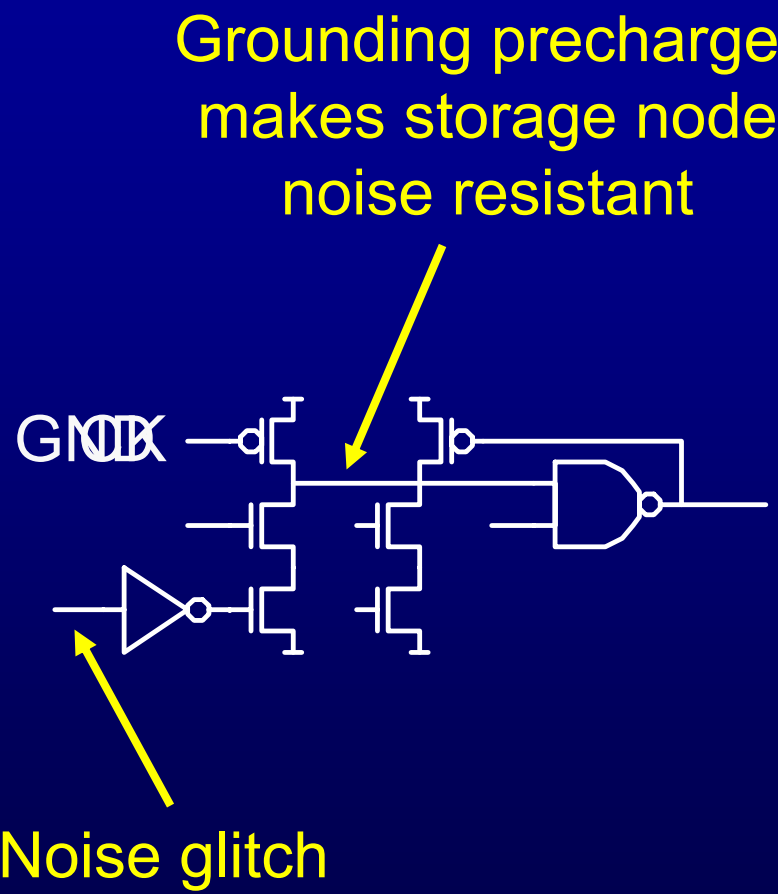
Lack of precharge in probing?

Root Causes

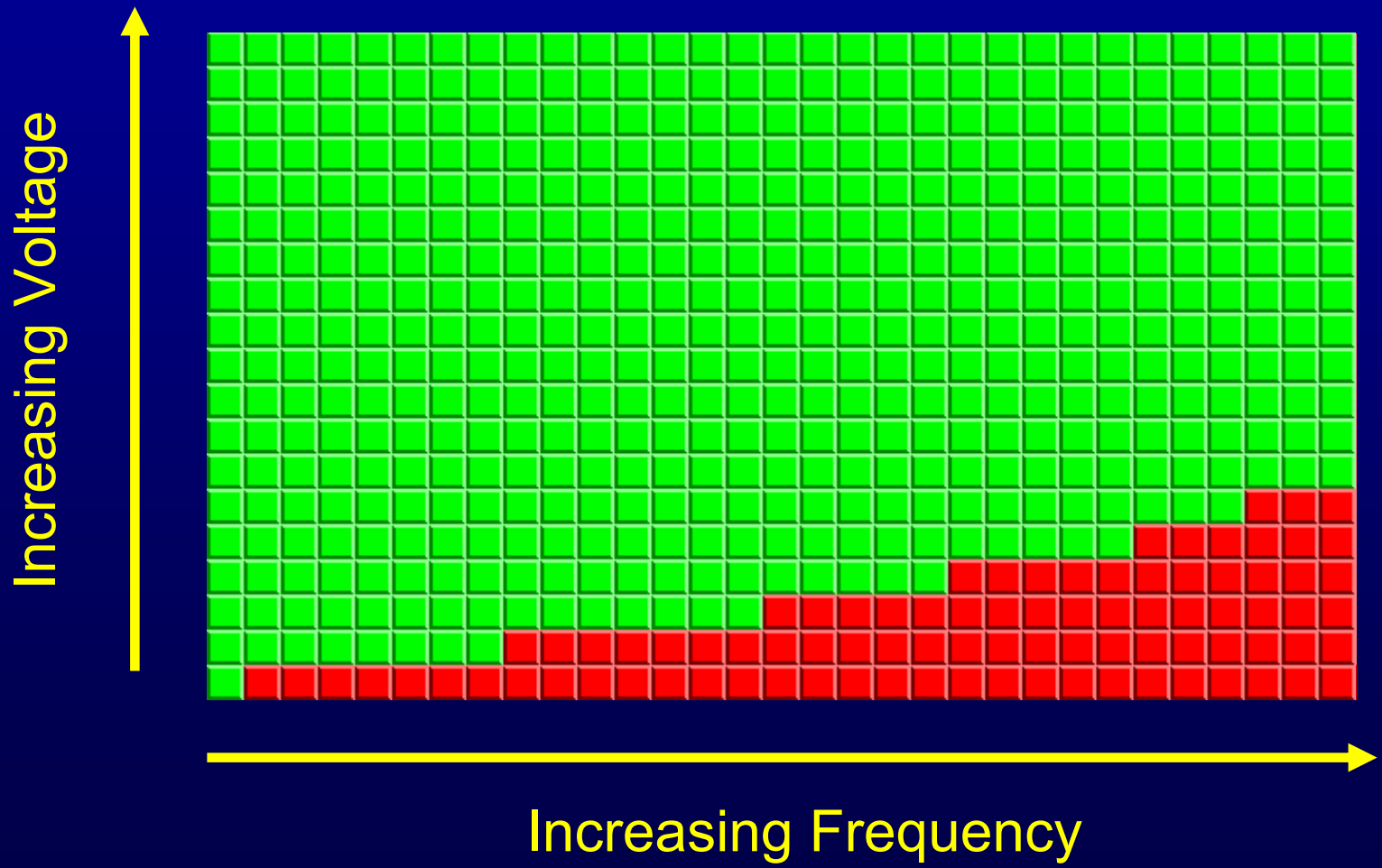

Weak precharge
Charge sharing
Noise
Lack of clocked evaluate FETs (drive fight)

FIB to the Rescue

- A fix is proposed
  - Convert the circuit to pseudo-NMOS
  - Provides noise resistance and addresses precharge and charge sharing
  - Little speed impact
- A FIB edit was performed to test the fix...



Before... and after!



Conclusion - Future Challenges

- Power control
  - Thermal issues
  - Variable operation per part/between parts
- High-speed interfaces
  - 2-4 GT/s with high pin counts
  - Beyond ATE capabilities for processors!
- Repeatability
- Process variation/lithography